CLAIMS

What is claimed is:

1. A processor comprising:

a first voltage supply input port to receive a first voltage at a first voltage level;

a second voltage supply input port to receive a second voltage;

a core to be powered by the first voltage; and

a memory region to be powered by the second voltage, the memory region to store at least a portion of a state of the processor while the first voltage supply is at a second voltage level.

2. The processor of claim 1, wherein the second voltage level is lower than the first voltage level.

3. The processor of claim 1, wherein the second voltage level is approximately 0 volts.

4. The processor of claim 1, further comprising an L2 cache to be powered by the first voltage.

5. The processor of claim 1, further comprising a first cache to be powered by the first voltage, and a second cache to be powered by the second voltage.

6. The processor of claim 5, further comprising a snoop controller to be powered by the second voltage, the snoop controller to snoop the second cache while the first voltage supply is at the second voltage level.

7. The processor of claim 5, wherein the second voltage level is a voltage level that causes a processor state to be lost.

8. The processor of claim 1, wherein the memory region is a portion of a cache of the processor.

9. A computer system comprising:

a fist voltage regulator to supply a first voltage at a first voltage level during a first period of time and at a second voltage level during a second period of time;

a second voltage regulator to supply a second voltage; and

a processor including a core to be powered by the first voltage and a memory region to be powered by the second voltage, the memory region to store at least a portion of a state of the processor during the second period of time.

10. The computer system of claim 9, wherein the second voltage level is less than half the first voltage level.

11. The computer system of claim 9, further comprising a clock to provide a clock signal to the processor, the clock signal to be on during the first period of time and off during the second period of time.

12. The computer system of claim 9, wherein the second period of time is associated with a low power state.

13. The computer system of claim 12, further comprising a cache to be powered by the second voltage, the cache to maintain its contents during the lower power state.

14. The computer system of claim 13, further comprising a snoop controller to be powered by the second voltage, the snoop controller to snoop the cache during the second period of time.

15. The computer system of claim 12, further comprising an L1 cache to be powered by the first voltage, the L1 cache to be flushed upon entering the lower power state.

16. The computer system of claim 9, wherein the portion of the state of the processor includes a strapping options register.

17. The computer system of claim 9, wherein the memory region is protected by error checking and correction (ECC) code.

18. A method comprising:

triggering a processor of a computer system to enter a low power state in which a first voltage supplied to a core of the processor is reduced to a level that causes a state of the processor to be lost; and

saving at least a portion of the state of the processor to a memory region of the processor upon entering the low power state, the memory region to be powered by a second voltage during the low power state.

19. The method of claim 18, further comprising flushing an L1 cache of the processor upon entering the low power state, the L1 cache to be powered by the first voltage.

20. The method of claim 18, further comprising maintaining contents of a cache of the processor upon entering the low power state, the cache to be powered by the second voltage.

21. The method of claim 20, further comprising performing a snoop of the cache during the low power state.

22. The method of claim 18, further comprising turning off a clock signal provided to the core upon entering the low power state.

23. A machine-readable medium including machine-readable instructions that, if executed by a machine, cause the machine to perform the method of claim 18.

24. A machine-readable medium including machine-readable instructions that, if executed by a machine, cause the machine to perform the method of claim 19.

25. A machine-readable medium including machine-readable instructions that, if executed by a machine, cause the machine to perform the method of claim 21.